

DIGITALLY ASSISTED ANALOG: REDUCING DESIGN CONSTRAINTS USING NONLINEAR DIGITAL SIGNAL PROCESSING

Batruni, Roy (Optichron, Inc., Fremont, CA USA, roy.batruni@optichron.com);
Ramachandran, Ravi (Optichron, Inc., Fremont, CA USA, ravir@optichron.com);
Ryan, Tim (Optichron, Inc., Fremont, CA USA, tim.ryan@optichron.com).

ABSTRACT

While Moore's Law has been predictive of continuous gains in digital circuit scaling, the relative performance of analog circuits has not scaled along with digital. Due to characteristics of analog circuitry, noise and distortion performance do not benefit from scaling, and some inherent challenges intensify with reduced supply voltage. Analog functions are often system roadblocks, resulting in constrained performance, especially in high-performance signal processing applications. However, as digital circuitry has scaled down, it has become practical to use digital processing in conjunction with analog functions to offload some of the bottlenecks, and the digitally assisted analog trend is well identified. This paper presents an example of the high leverage of this approach in overcoming a previously unsolvable problem: eliminating nonlinear distortion in a high-speed analog signal path using digital post-processing techniques. Through digital processing using advanced nonlinear signal processing algorithms, the ADC output signal is used as the input to a digitally replicated nonlinear transfer function. The output of this function is then subtracted from the ADC output in order to generate a highly linearized version of the ADC output and restore signal fidelity. The digital circuitry overhead is small for the implementation of the linearizer algorithms. In addition, the digitally assisted approach gives designers not only a much-valued linearity improvement, but also a greater command of the system design tradeoffs between speed, performance, power dissipation and cost. The ability to digitally correct for analog impairments in a high-speed analog-to-digital converter front end is a highly desirable feature in a Software Defined Radio application because it allows for higher input signal frequencies to be subsampled with low noise and high linearity.

1. INTRODUCTION

Nonlinear signal distortion is prevalent in RF receiver analog front-end architectures used in various applications such as medical imaging, scientific instrumentation and wireless communications. The same signal paths are also limited by noise impairments. In most applications, the goal is to build a system with the highest data rates and the largest number of channels at the lowest bit-error rates. This

means that the analog front end and the analog-to-digital converter technology in use must have the highest possible combination of bandwidth, signal-to-noise (SNR) ratio and spur-free dynamic range (SFDR). Such is the case in Software Defined Radio (SDR) architectures, where the aim is to capture as much of the signal bandwidth range at a high a sampling rate as possible – so that the functionality and configurability of the radio can then be undertaken by a software stack rather than by expensive and dedicated hardware for each type of radio.

In analog-to-digital converter front-end architectures, a number of such tradeoffs can be made between cost, bandwidth, power, SNR and SFDR. Design tradeoffs in the power, noise and linearity budget in this block can either constrain or relieve other parameter selection criteria in the RF portion of the signal front end. In this paper we examine several practical data converter and front-end interface design examples. We illustrate how cost, power, SNR and SFDR choices can be made using the concept of digitally assisted analog and in particular nonlinear digital signal processing, and how this can be of great benefit to the system design engineer.

2. ANALOG FRONT-END ARCHITECTURES

Figure 1 shows four different ADC analog front-end schemes, each with its own benefits and disadvantages. Figure 1a uses a Balun interface to the ADC, using passive components that provide the advantage of low cost and no power dissipation. The power dissipation of the whole system is around 700 m, due mainly to the power dissipation of the ADC (this does not include the nonlinear signal processor, which will be discussed later in the paper).

The main disadvantage is that this front end requires a high power level input signal of around 12 dBm in order for the ADC signal-to-noise ratio to benefit from the large signal dynamic range. In many applications this high input signal power is not possible, because the signal being quantized is not strong and needs to be amplified by active components. If in a given application such a large signal is available, this front end and ADC combination yields 72 dB of SNR and an average SFDR of 76 dBFS in the fourth Nyquist Zone.

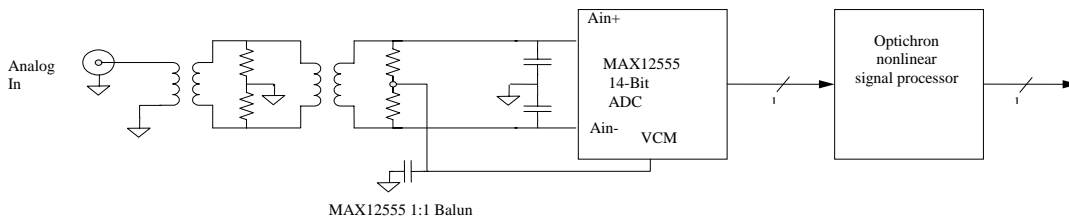


Figure 1a. BALUN front end for a commercially available Max12555 14-bit ADC with 91.5 MSPS cascaded with a nonlinear signal processing IC.

Figure 1b uses an AD8351 buffer amplifier interface to the ADC that has the advantage of medium cost and medium power dissipation of 150 mW, which keeps the overall system power consumption to around 850 mW (this does not include the nonlinear signal processor). This front end requires a medium power level input signal of around 5.7 dBm in order for the ADC signal-to-noise ratio to benefit from the large signal dynamic range. This front end and ADC combination yields 67.5 dB of SNR (the high gain of the amp results in amplifier noise gain) and an average SFDR of 55 dBFS in the fourth Nyquist Zone. As can be seen, the use of an active low-power amplifier has the advantage of lowering the required signal amplitude at the input of the analog front end, but it also results in a severe degradation in the SFDR.

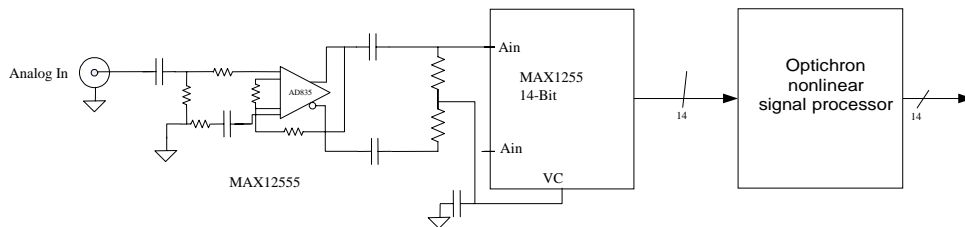


Figure 1b. Buffer amp front end using an AD8351 and a commercially available Max12555 14-bit ADC with 91.5 MSPS cascaded with a nonlinear signal processing IC.

Figure 1c uses a combination Balun and AD8351 amp, which enables a low-power input signal while keeping the low system cost and restricting front-end power dissipation down to 150 mW. The output of the ADC, however, is still encumbered by a low SFDR of 55 dBFS.

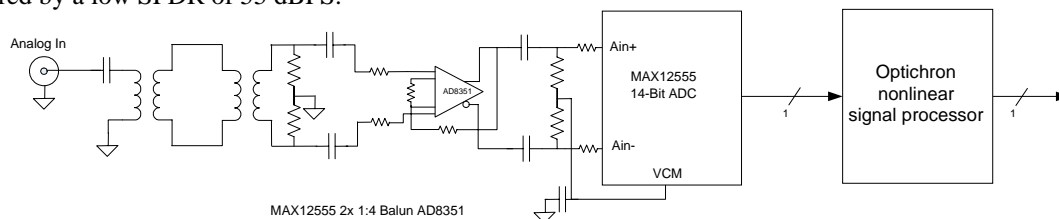


Figure 1c. BALUN-Buffer amp front end using an AD8351 and a commercially available Max12555 14-bit ADC with 91.5 MSPS cascaded with a nonlinear signal processing IC.

Figure 1d uses a low-noise AH22S amplifier, which has a power consumption of 1.5 W. While this arrangement enables a low input signal level and results in a higher SNR and SFDR (78 dB) at the output of the ADC, it comes at a cost of significantly higher power dissipation – caused mainly by the 1.5 W consumption in the amp alone.

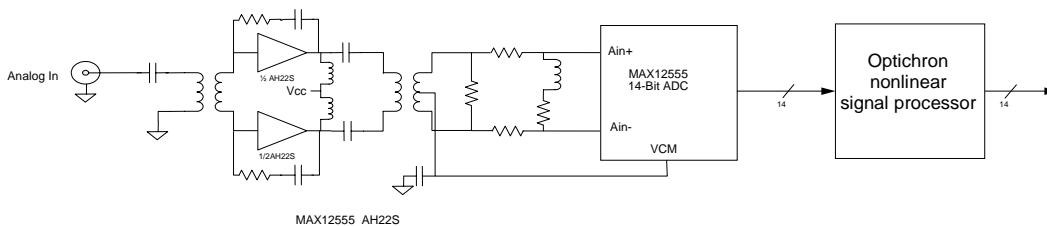


Figure 1d. Buffer amp front end using an AH22 and a commercially available Max12555 14-bit ADC with 91.5 MSPS cascaded with a nonlinear signal processing IC

Front End	Input Power (dBm)	SFDR (dBFS)	SNR (dB)	Power (W)
Max12555, Balun	12	76	72	0.7
Max12555, AD8351	5.7	55	67.5	0.85
Max12555, Balun + AD8351	-1.2	55	68.3	0.85
Max12555, AH22	-1.8	78	71.5	2.2

Table 1. Summary of four variations of analog-front-end interface to the Max12555 14-bit ADC in the fourth Nyquist Zone.

The results of all four variations of front ends are shown in Table 1. Clearly the most desirable architecture from a power consumption and input signal power requirement aspect is the third option of Balun + AD8351 combination. This, however, comes at a big sacrifice in SFDR and may not be a practical option as it stands. If, on the other hand, one requires a low input signal power, a medium-level SFDR and a good SNR, then the fourth option shown in Table 1 is the optimal choice, but that is achieved at considerably higher power consumption. The problem is magnified when a multi-channel system is being designed and the extra 1.5W of power dissipation grows by many more Watts.

4. DIGITALLY ASSISTED ANALOG

Digitally assisted analog is an emerging concept that makes use of Moore's Law in a manner where increased gate density and lowered cost of digital ICs allow for high throughput and low-power digital processing of signal attributes. These factors, in turn, can alleviate critically tight specifications on analog components when designing analog signal paths.

In one example, we show how selecting a lower power but higher distortion amp yields a raw signal with poor SFDR, but using digitally assisted analog to correct for the nonlinear distortion results in an overall system that has excellent linearity and low power. Another example shows how if high power consumption was not a system design constraint in some situations, a choice of a low-noise and high-power-consumption amp will result in a medium-level linearity and reasonably good SNR – and by using digitally assisted analog, the linearity can further be improved by 15 dB.

After that, we illustrate how digitally assisted analog, and specifically nonlinear digital signal processing, corrects for such signal impairments in the analog electronics. The examples below discuss the performance of a nonlinear digital signal processor designed by the authors that

targets nonlinear distortion generated in the buffer amplifier and the analog-to-digital converter. The advantages of such an approach are demonstrated to be both lower power consumption and a higher SFDR figure for the amp-ADC combination.

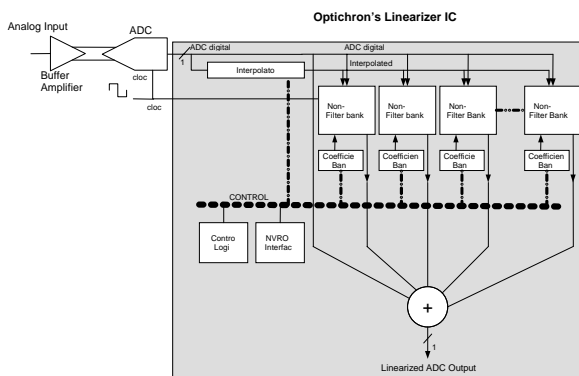
5. NONLINEAR DISTORTION

Nonlinear distortion is a naturally occurring phenomenon that pervades communications channels and analog electronics. Nonlinear distortion in analog electronics occurs when the signal input-output transfer function is governed by a higher-order polynomial. The distortion function may be static or dynamic, continuous or with discontinuities. The result is an output that contains the fundamental components of the input signal as well as harmonics that are images at multiples of the signal fundamental frequencies.

The main difficulty with correcting for nonlinear distortion is that once the transfer function deviates from a linear surface there are no constraints on what shape it can take, and therefore the variations are infinite. In applications such as the ones discussed in this paper nonlinear distortion comprises dynamically varying components in the buffer amplifier as well as static and discontinuous components generated in the ADC sampled-data pipe.

Further complicating the ability to model and correct for nonlinear distortion is the fact that, in many applications, input signal frequencies are at a high Nyquist Zone and are then subsampled by the ADC to the first Nyquist Zone. This results in the loss of information, because signal history plays a role in dynamic nonlinearities and subsampling results in significant loss of signal history. Other important factors that make this problem difficult to solve are that most dynamic nonlinearities are a function of signal slew-rate and the signal subsampling degrades the ability to estimate that factor.

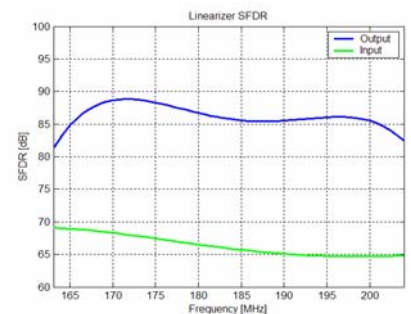
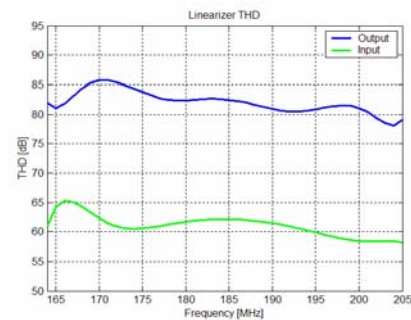
Figure 2 below illustrates the block diagram of a custom nonlinear signal processing architecture designed by the authors that addresses the problems inherent in nonlinearly distorted subsampled signals in general, as well as signals in analog-to-digital applications in particular. The engine shown here consists of 16 nonlinear filtering modules that can be configured to handle different types of distortion: static, dynamic, dispersive, discontinuous and combinations thereof. One major module in this engine is a linear interpolator that digitally replicates an estimate of the input signal at the relevant Nyquist Zone. The output of the interpolation block is used by the different nonlinear modules when estimating dynamic- and slew-rate-dominated nonlinear components. Each nonlinear module processes the ADC digital output and partial information from the interpolation block to generate partially linearized signal estimates. The summation of the 16 nonlinear filter outputs results in a linearized ADC output such that the ADC signal-to-noise ratio is not degraded. This is achieved by using nonlinear prediction techniques where estimates of the nonlinear components are subtracted from the ADC signal. No feed-through filtering of the ADC signal is performed, and thus the ADC signal SNR is unaltered.



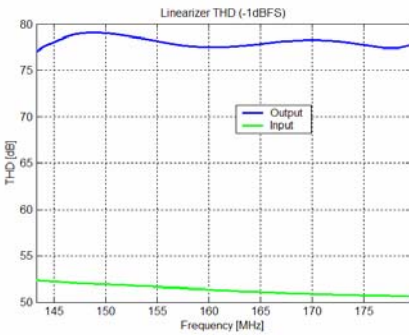
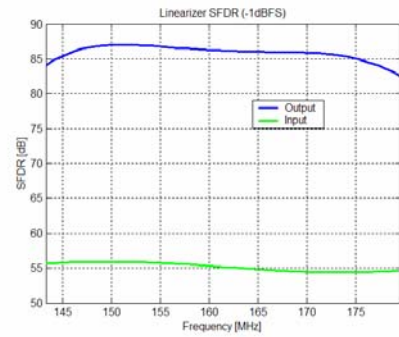
6. DIGITALLY ASSISTED ANALOG AND NONLINEAR SIGNAL PROCESSING: SYSTEM BENEFITS

The benefits accruing from utilizing the digitally assisted analog concept are not restricted to simply achieving higher linearity. As will be illustrated in this section, other system-wide benefits, such as lower power and cost, result as well. Advanced, agile and flexible digital signal processing benefits from the high density and low cost of the continually advancing digital technologies to remove nonlinear distortion. Use of such digital signal processing enables the choice of not only low-power buffer amplifier front ends, but also low-power analog-to-digital converters that inherently have higher nonlinear distortion.

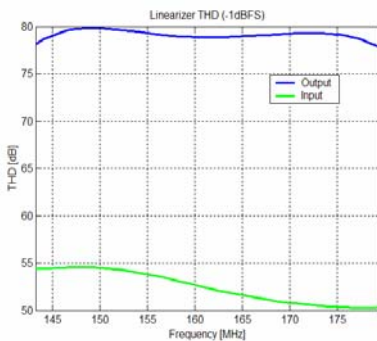
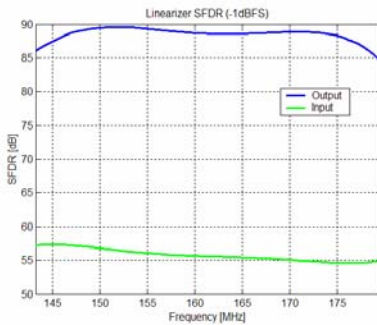
While the analog front-end block diagrams shown above use a certain type of ADC from one manufacturer, the linearization integrated circuit was designed by the authors to work with any analog-to-digital converter. Shown below are performance results with input signals in the fourth Nyquist Zones with a variety of ADCs from several manufacturers. The ability to choose a particular ADC based on slight variations in SNR or power dissipation, while maintaining the high linearity using the nonlinear signal processing engine, is another system benefit that designers can use to their advantage.



Performance with the AD6645 ADC and AD8351 amp.

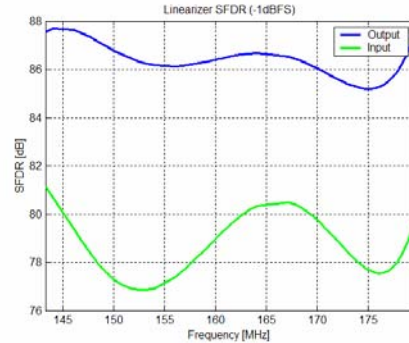


Performance with the LTC2299 ADC and AD8351 amp.

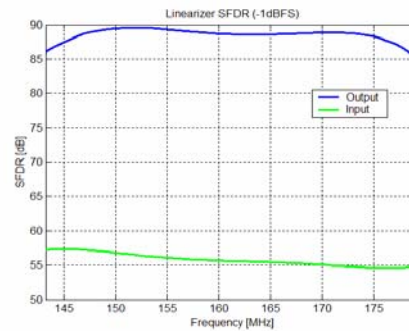


Performance with the Max12555 ADC and AD8351 amp.

Green plots show Amp-ADC output Total Harmonic Distortion and Spur Free Dynamic Range before Optichron's Linearizer IC with input frequencies in the 4th Nyquist Zone, using the analog-to-digital converters AD6645, LTC2299 and Max12555 respectively. Blue Plots shows the same plots after Optichron's Linearizer IC. Optichron's linearization technology is universal. Performance is independent of the source or type of nonlinearity.



Performance improvement using Max12555 ADC and AH22 buffer. Power dissipation of the AH22 is 1.5W. Total power dissipation is 3W.



Performance improvement using Max12555 ADC and AD8351 buffer. Power dissipation of the AD8351 is 0.15W. Total power dissipation is 1.6W.

Optichron's Linearizer IC allows designers to achieve the highest linearity out of the signal path at a lower cost and power dissipation. The plot on the left is the case where a Watkins Johnson AH22 that has a power dissipation of 1.5W is used. Raw SFDR is in the 78 dB range. The plot on the right uses the AD8351 amp with a raw SFDR of 55 dB but a power dissipation of 0.15W. By using Optichron's Linearizer IC the performance of both systems is in the 85 dB range, but the one on the left has a power dissipation of 3W and the one on the right 1.6W.

In Table 2, the performance of the different front-end options is shown when the nonlinear signal processing engine designed by the authors is used to cancel the nonlinear distortion arising from the buffer amp and the ADC. The digital engine allows for all of the different options to have roughly the same linearity. System designers can then chose other attributes that differentiate the system parameters, such as power dissipation vs. signal-to-noise ratio, or input signal power vs. signal-to-noise ratio, and so on. If power dissipation is the biggest constraint in the system under design, then clearly option 3 is most desirable since it combines high linearity, low input signal power requirements and low overall power dissipation while sacrificing 3 dB in SNR. If maximum SNR and SFDR are highly desired while requiring low input signal power, then option 4 is more desirable, and this option improves the SFDR by 12 dB over the option of not using the nonlinear signal processing engine.

Front End	Input Power (dBm)	SFDR (dBFS)	SNR (dB)	Power 0.18u Engine (W)	Power 0.13u Engine (W)
Max12555 , Balun	12	92	72	1.5	1
Max12555 , AD8351	5.7	90	67.5	1.65	1.15
Max12555 , Balun + AD8351	-1.2	90	68.3	1.65	1.15
Max12555 , AH22	-1.8	90	71.5	3.0	2.5

Table 2. Summary of four variations of analog-front-end interface to the Max12555 14-bit ADC cascaded with Optichron’s nonlinear signal processor IC. Power consumption numbers for the analog front end, ADC and with the 0.18u version of the nonlinear signal processor and with the 0.13u version are shown.

7. CONCLUSION

Digitally assisted analog is an emerging trend that combines attractive features of high-performance analog circuits with advanced digital processing. The resulting combination provides a boost in performance along with a reduction in system constraints such as power dissipation, cost and input dynamic range. Making use of the vast flexibility in algorithms that digital processing allows – as well as the ever-shrinking size, power and cost of digital circuitry – is becoming a more commonplace practice for system designers. The examples illustrated in this paper show clearly that using a powerful nonlinear signal processing integrated circuit can cut down the power dissipation by several Watts in a system design and even more so in certain systems, when several channels of an analog front end are being used. Differences between 0.18u and 0.13u power dissipation for the digital engine illustrate why this trend of digitally assisted analog will be more attractive in the future as smaller-geometry digital processes become even more attractive from a cost point of view.

REFERENCES

- [1] W.J. Rugh, Nonlinear System Theory: The Volterra/Weiner Approach, Johns Hopkins University Press, Baltimore, MD, 1981.
- [2] J. Tsimbinos, “Identification and Compensation of Nonlinear Distortion,” Ph.D. Thesis, University of South Australia, 1995.
- [3] D. Hummels, “Linearization of ADCs and DACs for All-Digital Wide-Bandwidth Receivers,” 4th Workshop on ADC Modeling and Testing, Bordeaux, France, September 1999.
- [4] J.H Larrabee, D.M. Hummels, F.H. Irons, “ADC Compensation Using a Sin Wave Histogram Method,” IEEE Instrumentation and Measurement Technology Conference, Ottawa, Canada, May 1997.